CHANGES TO THE SPECIFICATION

Please insert the following paragraph immediately following the title of the application:

--CROSS REFERENCE TO RELATED APPLICATIONS

The present application is a continuation application of United States Patent Application No. 10/094,804, filed on March 12, 2002, which in turn is a continuation of U.S. Patent Application No. 09/386,505, filed August 31, 1999 (now U.S. Patent No. 6,380,787, issued on April 30, 2002), the disclosures of which are herewith incorporated by reference in their entirety.--

Please rewrite the paragraph found beginning on page 24 at line 15 and ending on page 25 at line 6 as follows:

Node 1 couples the drain region, 821 and 822, for the first and the second transistor, M1 and M3, in the first amplifier 810 to gates, 840 and 841, of the second transistor, M3 and M4, in the first and the second amplifier 810 and 820. The first and second transistors, M2 and M4, of the second amplifier 820 are coupled at a drain region, 823 and 824 respectively. In the embodiment shown in FIG. 11A, a signal output node 2 is coupled to the drain region, 823 and 824, of the first and the second transistor, M2 and M4, in the second amplifier 820. In an alternative embodiment, the signal output node ~~2~~ can be coupled (at reference number 1) to the drain region, 821 and 822, of the first and the second transistor, M1 and M3, in the first amplifier 810. As shown in FIG. 11A the signal output node is further coupled to a gate ~~880~~ 830 of a third transistor M8. In one embodiment, the third transistor M8 is an n-channel metal oxide semiconductor (NMOS) transistor M8. Each amplifier, 810 and 820, includes a signal input node, 5 and 4 respectively, which is coupled to a source region, 825 and 826, of the first transistor, M1 and M2.